Practice on LabVIEW and HIL for Power Electronics and Drives applications

A. Lidozzi, M. di Benedetto

Monday July 18th 11.00-13.00 and 14.00-17.45 (GMT+1)
Tuesday July 19th 09.15-13.00 and 14.00-17.45
Wednesday July 20th 09.15-13.00 and 14.00-16.30

Introduction

Nowadays, even a common power converter can exhibit an increased number of active devices and higher switching frequency than ever to satisfy a higher control performance demand. This results in an increased complexity related to the control board, where usually a combined μC (or μP, DSP) and FPGA are both installed. Those two 'actors' require a completely different programming approach and development tools from those utilized by traditional boards.
Accordingly, control algorithm development is considered a 'time consuming' task within a research or industrial project. The Integrated Development Environments provided by the control platforms manufacturers or third parties, are constantly moving from the classical, old, text-based approach to a new, fast and simple to learn graphical programming method. Moreover, a high level of abstraction is usually demanded to accelerate the learning time even on non-specialist workers. However, a full control on the hardware is still mandatory.
The course will cover the methodologies to switch to new graphical programming development environments, starting from a review and going into the most promising solutions.
Code splitting between targets, best practices, and code efficiency will be part of the tutorial.

Outline

Theory and practice with the National Instruments sbRIO-9651 and Linux real-time OS. Insight view and develop of specific Power Electronics and Drives applications using LabVIEW integrated development environment.

- LabVIEW basic concepts, front panel, and block diagram, debugging, programming guidelines. Application development. Graphical programming of the Real-Time and FPGA targets. Communication between targets. Code efficiency and best practices.
- Development of the FPGA main scheduler and synchronization with the on board μProcessor, PWM modulator with configurable dead-time.
- Floating-point math operations on FPGA target. (*a must have!*)
- Development on the FPGA target of high-performance control algorithms such as repetitive control, resonant controllers, Model Predictive Control, and combined control structures. Code splitting between targets. Insight view of PWM modulators for multilevel power converter topologies, dead-time generation, and safe turn-off.
- Closed loop tests with Real-Time Hardware-In-the-loop simulators (Typhoon, National Instruments and OPAL-RT eHS solver)
    - Creating HIL personalities for different converter topologies
    - Simulation time-step and accuracy
- Discussion on the lab sessions.

Control board info: www.ped-board.com

Class can be attended on-line and in person. No fees for the attendees. To register, send an email to alessandro.lidozzi@uniroma3.it

Alessandro Lidozzi *received the Electronic Engineering degree and the Ph.D. degree from the Roma Tre University, Rome, Italy, in 2003 and 2007, respectively. Since 2017, he has been Associate Professor with the C-PED, ROMA TRE University. His research interests are mainly focused on power converters and electrical machines modeling and control, Hardware-In-the-Loop simulators and Power-Hardware-In-the-Loop emulators, graphical programming of FPGA and development of high-performance control platforms based on combined DSP-FPGA targets.*
Marco di Benedetto *received the M.Eng. degree in electronic engineering from the University of Roma Tor Vergata, Rome, Italy, in 2014, and the Ph.D. degree in mechanical and industrial engineering from the Roma Tre University, Rome, Italy, in 2018. Since November 2018, he has been a Research Fellow with the Center of Power Electronics and Drives, Roma Tre University. His research interests are mainly focused on hardware and FPGA control design for multilevel power converter topologies.*

Venue
ROMA TRE University, Department of Engineering. Via Vito Volterra 62, 00146 Roma (Italy)
Room: N8

How to reach us
By CAR
University parking lots are available in Via della Vasca Navale 107. https://goo.gl/maps/tMiJQNYDttreDw7j8

By subway
From the train station *Roma Termini*, *Line B* direction *Laurentina*, stop *Basilica di San Paolo*. The Department of Engineering is at walking distance: Via Vito Volterra 62.